

Amendments to the Claims:

Please use the following listing of claims to replace all prior versions, and listings, of the claims in the above-identified application.

Listing of Claims:

CLAIM 1 (original)

- 1 A method for fabricating complementary vertical bipolar junction transistors comprising the
2 steps of:
- 3 providing a sapphire substrate;
 - 4 forming a layer of silicon on said sapphire substrate;
 - 5 recrystalizing said silicon layer;
 - 6 forming a P+ region in said silicon layer to become a collector for a PNP transistor;
 - 7 forming N+ region in said silicon layer to become a subcollector for an NPN transistor;
 - 8 forming an N silicon layer over said P+ and N+ regions to become an intrinsic base
9 region for said PNP transistor and to become a collector region for said NPN transistor;
 - 10 forming islands of what is to become said PNP transistor and of what is to become said
11 NPN transistor by removing any silicon therebetween to said sapphire substrate;
 - 12 forming a P intrinsic base region in said N collector region for said NPN transistor;
 - 13 forming P+ extrinsic base regions in said P intrinsic base region for said NPN transistor;
 - 14 forming a P+ emitter region in said N base region for said PNP transistor;

15 forming an N⁺ emitter region on said P base region for said NPN transistor;
16 forming N⁺ extrinsic base regions in said N base region for said PNP transistor; and
17 forming individual conducting metal contacts with said emitters and extrinsic bases, said
18 individual conducting metal contacts being formed between oxide regions.

CLAIM 2 (original)

1 The method according to claim 1 wherein said recrystallization is done by a double solid phase
2 epitaxy technique.

CLAIM 3 (original)

1 The method according to claim 1 wherein said silicon layer formed on said sapphire substrate is
2 approximately 0.3 micrometers thick.

CLAIM 4 (original)

1 The method according to claim I wherein said N, N⁺, P and P⁺ regions are created through ion
2 implantation.

CLAIM 5 (original)

1 The method according to claim 1 wherein said α -type silicon layer is approximately 2.5
2 micrometers thick.

CLAIM 6 (original)

- 1 The method according to claim 1 wherein arsenic ion implantation is used to produce said –type
2 and N+-type regions.

CLAIM 7 (original)

- 1 The method according to claim 1 wherein boron ion implantation is used to produce said P-type
2 and P+-type regions.

CLAIM 8 (previously presented)

- 1 The method of claim 1 further including the steps of:
2 forming a P+ collector plug region in said N base region for said PNP transistor so that
3 said P+ collector plug region is incorporated into said P+ collector for said PNP transistor;
4 forming an N+ collector plug region in said P intrinsic base region for said NPN
5 transistor so that said N+ collector plug region is incorporated into said N collector region of said
6 N+ sub-collector region for said NPN transistor;
7 forming individual conductive metal contacts with said collector plug regions; and
8 forming an oxide region between said collector plug metal contacts.

CLAIM 9 (original)

- 1 The method according to claim 8 wherein said N, N+, P and P+ regions are created through ion
2 implantation.

CLAIM 10 (original)

- 1 The method according to claim 8 wherein arsenic ion implantation is used to produce said N-type
- 2 and N+-type regions.

CLAIM 11 (original)

- 1 The method according to claim 8 wherein boron ion implantation is used to produce said P-type
- 2 and P+-type regions.